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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,253	03/10/2004	Hiroshige Hirano	MTS-2101US3	5368
23122	7590	07/22/2004	EXAMINER	
RATNERPRESTIA P O BOX 980 VALLEY FORGE, PA 19482-0980			TRA, ANH QUAN	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 07/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/797,253

Applicant(s)

HIRANO ET AL.

Examiner

Quan Tra

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 10 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 15-17,20 and 21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 15-17,20 and 21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☒ Certified copies of the priority documents have been received in Application No. 08/817,746.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 03/10/04.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date: \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 15 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 15 is not enable because it is a single means claim. See MPEP 2164.08a and *In re Hyatt*, 708 F.2d 712, 714-715, 218 USPQ 195, 197 (Fed. Cir. 1983).

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 15-17, 20 and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 15 is misdescriptive, thereby renders the claim indefinite. It is misdescriptive to recite the power power on reset circuit comprising "a voltage detection circuit which detects a first voltage and a second voltage". Figure 17 shows the power on reset circuit detecting when the power supply reaches the first voltage and the second voltage or when the power supply falls below the first and second voltages. Figure 17 does not shows the power on reset circuit detect the first and second voltages. It is also misdescriptive to recite "the first signal being transmitted

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at the second voltage...when the power supply voltage drops". Figure 18 does not shows signal D21 perform such function. It is unclear where the operational sequence occur.

A similar reasons for claims 16, 17, 20 and 21. As further called in for claimed 20, there is no antecedent basis for the limitation "the third voltage" in line 10.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by McClintock (USP 5612642).

Insofar as understood to claim 15, McClintock's figures 1-2 show a power-on/off reset circuit characterized by comprising a voltage detection circuit which detects a first voltage (VPOR2) and a second voltage (VPOR1) higher than the first voltage, and outputs a first signal (POR), the first signal being transmitted at the second voltage when a power-supply voltage rises, and transmitted at the first voltage when the power-supply voltage drops. It is seen as an intended use for using McClintock's power on reset circuit for preventing a new operational sequence of the other circuit when the power-supply voltage is equal to or lower than a voltage for the first signal to be transmitted (as best understood, the operational sequence occurs outside the power on reset circuit).

As to claim 20, figure 4 shows a semiconductor device comprising a non-volatile memory (404) and a power-on/off reset circuit (406) including a voltage detection (figure 2) circuit which detects a first voltage (VPOR2) and a second voltage (VPOR1) higher than the first voltage and outputs a first signal (POR), the first signal being transmitted at the second voltage when a power-supply voltage rises, and transmitted at the first voltage when the power-supply voltage drops, and preventing a new operational sequence when the power-supply voltage is equal to or lower than a voltage for the first signal to be transmitted, wherein the semiconductor device is characterized by not operating the non-volatile memory when the power-supply voltage is equal to or lower than the first voltage or equal to or lower than the third voltage (column 3, line 58-column 4, line 25).

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 16, 17 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over McClintock (USP 5612642).

As to claims 16 and 21, McClintock's figures 1 and 2 shows all limitations of the claim except for a second voltage detection circuit which detect a third voltage. However, it would have been obvious to one having ordinary skill in the art to duplicate the circuit figure 2 and figure 4 because it has been held that mere duplication of parts has no patentable significance unless a new and unexpected result is produced. See *In re Harza*, 274 F.2d 669, 124 USPQ 378

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(CCPA 1960). Thus, the newly added circuit is the second voltage detection circuit which detect a third voltage (VPOR2 of the newly added circuit) lower than the first voltage. As further called in for claim 21, the newly added POR circuit 406 is also disable the newly added memory circuit 404 when the power supply falls below the third voltage (VPOR2 of the newly added circuit).

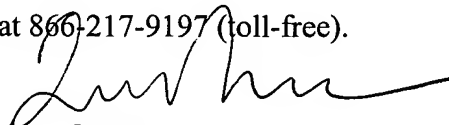
As further called in to claim 17, it is seen as an intended use and matter of design preference for selecting a time for a power supply voltage to drop from the first voltage to the third voltage being longer than a predetermined operation sequence completion time.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Quan Tra  
Patent Examiner

July 21, 2004